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EXAMINER	
VU, QUANG D	

ART UNIT	PAPER NUMBER
2811	

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Please find below and/or attached an Office communication concerning this application or proceeding.

PTO-90C (Rev. 10/03)

Office Action Summary	Application No. 09/828,862	Applicant(s) IMAI, KIYOTAKA
	Examiner Quang D Vu	Art Unit 2811

-- *The MAILING DATE of this communication appears on the cover sheet with the correspondence address* --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If the period for reply specified above is less than thirty (30) days, a reply within the statutory minimum of thirty (30) days will be considered timely.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *08 September 2004*.

2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *3-22* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *3-22* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☐ The drawing(s) filed on _____ is/are: a)☐ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☒ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☒ All b)☐ Some * c)☐ None of:

1.☒ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☐ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☐ Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08) Paper No(s)/Mail Date _____.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____.
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other: _____.

DETAILED ACTION

Claim Rejections - 35 USC § 103

1. The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

2. Claims 3-7, 14 and 18-21 are rejected under 35 U.S.C. 103(a) as being unpatentable over US Patent No. 5,880,500 to Iwata et al.

Regarding claim 3, Iwata et al. (figure 1) teach a method for manufacturing a semiconductor device comprising:

implanting n-type impurities within an MMOSFET forming region during a formation of channel regions and n-type source/drain regions (n-type source/drain [108]; column 9, line 17);

Iwata et al. teach p-type channel region (see figure1). Therefore, it is inherently teach implanting boron ions (p-type) for forming a channel region to adjust threshold voltage within the NMOSFET forming region divided by an element dividing region;

implanting two different ions after the implantation of boron, comprising:

implanting arsenic ions in a semiconductor substrate (100) at a first acceleration energy level thereby forming the source/drain regions (108) within the NMOSFET forming region (column 11, lines 8-15);

implanting phosphorous ions at a second acceleration energy level (column 10, line 66 – column 11, line 3) lower than the first acceleration energy level; and

performing a heat treatment to active the arsenic ions and the phosphorous ions in the ion-implanted regions to form source/drain regions and buffer regions, the buffer regions comprising phosphorous ions and extending beyond the source/drain regions (column 10, line 66 – column 12, line 45). It is inherent that suppressing transient enhancement diffusion of boron implanted region.

It is inherent that the arsenic ion implanted regions suppress a reverse short channel effect in the NMOSFET.

Since first acceleration energy level (50 keV) of the arsenic ions is greater than the second acceleration energy level (30keV) of the phosphorous ions, the concentration peak of the phosphorous ions would locate in the arsenic ion implanted regions.

Iwata et al. differ from the claimed invention by not showing after the implanting the arsenic ions, continuously implanting phosphorous ions in the arsenic ion implanted regions. It would have been obvious to one having ordinary skill in the art at the time the invention was made to select the order of forming. See Ex parte Rubin , 128 USPQ 440 (Bd. App. 1959) (Prior art reference disclosing a process of making a laminated sheet wherein a base sheet is first coated with a metallic film and thereafter impregnated with a thermosetting material was held to render prima facie obvious claims directed to a process of making a laminated sheet by reversing the order of the prior art process steps.). See also In re Burhans, 154 F.2d 690, 69 USPQ 330 (CCPA 1946) (selection of any order of performing process steps is prima facie obvious in the absence of new or unexpected results); In re Gibson, 39 F.2d 975, 5 USPQ 230 (CCPA 1930) (Selection of any order of mixing ingredients is prima facie obvious.).

Regarding claim 4, Iwata et al. teach implanting n-type impurities are implanted to form an n-type extension region (impurity diffusion region [107]) before the implanting the two different ions (the arsenic and phosphorous implanting) (column 10, lines 53 – 65).

Regarding claim 5, Iwata et al. teach an acceleration energy and a dosage of the phosphorous ion are determined such that an ion-implanted region (105) of the phosphorous ion extends beyond a bottom surface of an ion-implanted region (108) of the arsenic ion. It is inherent that a dosage of the arsenic ion is determined to obtain electrical characteristics for the NMOSFET.

Regarding claim 6, Iwata et al. differ from the claimed invention by not showing the acceleration energy of the arsenic ion is not greater than 15 keV, and the acceleration energy of the phosphorous ion is not greater than 15 keV. It would have been obvious to one having ordinary skill in the art at the time the invention was made for the acceleration energy of the arsenic ion is not greater than 15 keV, and the acceleration energy of the phosphorous ion is not greater than 15 keV in order to reduce the reverse short channel effect. Furthermore, it has been held that where the general conditions of a claim are disclosed in the prior art, discovering the optimum or workable ranges involve only routine skill in the art. In re Aller, 105 USPQ 233.

Regarding claim 7, Iwata et al. differ from the claimed invention by not showing the dosage of the arsenic ion is between $2 \times 10^{15}/\mathrm{cm}^2$ and $1 \times 10^{16}/\mathrm{cm}^2$, and the dosage of the phosphorous ion is between $5 \times 10^{14}/\mathrm{cm}^2$ and $1 \times 10^{15}/\mathrm{cm}^2$. It would have been obvious to one having ordinary skill in the art at the time the invention was made for the dosage of the arsenic ion is between $2 \times 10^{15}/\mathrm{cm}^2$ and $1 \times 10^{16}/\mathrm{cm}^2$, and the dosage of the phosphorous ion is between $5 \times 10^{14}/\mathrm{cm}^2$ and $1 \times 10^{15}/\mathrm{cm}^2$ in order to reduce the reverse short channel effect. Furthermore,

it has been held that where the general conditions of a claim are disclosed in the prior art, discovering the optimum or workable ranges involve only routine skill in the art. In re Aller, 105 USPQ 233.

Regarding claim 14, Iwata et al. differ from the claim invention by not showing the first acceleration energy level comprises about 10 keV or less. It would have been obvious to one having ordinary skill in the art at the time the invention was made for the first acceleration energy level comprises about 10 keV or less in order to reduce the reverse short channel effect. Furthermore, it has been held that where the general conditions of a claim are disclosed in the prior art, discovering the optimum or workable ranges involve only routine skill in the art. In re Aller, 105 USPQ 233.

Regarding claim 18, Iwata et al. teach the boron ions (column 10, lines 53-57) are implanted in the semiconductor substrate (100) to form a well region (109), the arsenic ions (108) being implanted in the well region of the semiconductor substrate.

Regarding claim 19, Iwata et al. differ from the claimed invention by not showing the boron ions are implanted in the well region of the semiconductor substrate to form the channel region in the embodiment of figure 1. However, Iwata et al. teach the boron ions (column 16, line 66 – column 17, line 9) are implanted in the well region of the semiconductor substrate to form the channel region in the embodiment of figures 6a-m. It would have been obvious to one having ordinary skill in the art at the time the invention was made to include claimed limitation shown in the embodiment of figures 6a-m into the embodiment of figure 1, since it is desirable for them to have functionality. The combined device shows implanting boron ions in the well region of the semiconductor substrate to form a channel region.

Regarding claim 20, the combined device differs from the claimed invention by not showing implanting boron ions to form the channel region comprises implanting boron ions at 30 keV at a dose 1.0 x $10^{13}/cm^2$. It would have been obvious to one having ordinary skill in the art at the time the invention was made for implanting boron ions to form the channel region comprises implanting boron ions at 30 keV at a dose 1.0 x $10^{13}/cm^2$ in order to reduce the reverse short channel effect. Furthermore, it has been held that discovering an optimum value of a result effective variable involves only routine skill in the art. In re Boesch, 617 F.2d 272, 205 USPQ 215 (CCPA 1980).

Regarding claim 21, the combined device shows forming a gate electrode on the channel region; implanting arsenic ions in the well region to form extension regions; performing a heat treatment (column 17, lines 56-64) to activate the arsenic ions in the well region; and after the performing the heat treatment, forming side walls on the gate electrode.

3. Claims 8-13, 15-17 and 22 are rejected under 35 U.S.C. 103(a) as being unpatentable over US Patent No. 5,880,500 to Iwata et al. in view of US Patent No. 6,649,308 to Wu.

Regarding claim 8, Iwata et al. (figure 1) teach a method for manufacturing a semiconductor device comprising:

implanting arsenic ions in a semiconductor substrate (100) at a first acceleration energy level to form an arsenic ion implanted region (108) (column 11, lines 8-15);

implanting phosphorous ions in the arsenic ion implanted region (impurity diffusion region [108]) at a second acceleration energy level (column 10, line 66 – column 11, line 3) lower than the first acceleration energy level; and

performing a heat treatment to activate the arsenic ions and phosphorous ions to form an n-type source/drain main region (108) comprising arsenic and phosphorous ions (column 11, line 59 – column 12, line 45), and an n-type source/drain buffer region (105) comprising phosphorous ions, the n-type source/drain buffer region (105) extending beyond the n-type source/drain main region (108).

Iwata et al. differ from the claimed invention by not showing after the implanting the arsenic ions, implanting phosphorous ions in the arsenic ion implanted regions. It would have been obvious to one having ordinary skill in the art at the time the invention was made to select the order of forming. See Ex parte Rubin , 128 USPQ 440 (Bd. App. 1959) (Prior art reference disclosing a process of making a laminated sheet wherein a base sheet is first coated with a metallic film and thereafter impregnated with a thermosetting material was held to render prima facie obvious claims directed to a process of making a laminated sheet by reversing the order of the prior art process steps.). See also In re Burhans, 154 F.2d 690, 69 USPQ 330 (CCPA 1946) (selection of any order of performing process steps is prima facie obvious in the absence of new or unexpected results); In re Gibson, 39 F.2d 975, 5 USPQ 230 (CCPA 1930) (Selection of any order of mixing ingredients is prima facie obvious.).

Iwata et al. further differ from the claimed invention by not showing the first acceleration energy is no greater than 15keV. The energy of implanting arsenic ions is a known variable, which is subject to routine experimentation and optimization. Wu teach the implanting arsenic ions at the acceleration energy about 5 to 150keV (column 4, lines 42-48), which is in the claimed range. It would have been obvious to one having ordinary skill in the art at the time the invention was made for the first acceleration energy is no greater than 15keV in order to reduce

the reverse short channel effect. Furthermore, it has been held that discovering an optimum value of a result effective variable involves only routine skill in the art. In re Boesch, 617 F.2d 272, 205 USPQ 215 (CCPA 1980).

Iwata et al. and Wu differ from the claimed invention by not showing the second acceleration energy is no greater than 10 keV. It would have been obvious to one having ordinary skill in the art at the time the invention was made for the second acceleration energy is no greater than 10 keV in order to reduce the reverse short channel effect. Furthermore, it has been held that discovering an optimum value of a result effective variable involves only routine skill in the art. In re Boesch, 617 F.2d 272, 205 USPQ 215 (CCPA 1980).

Regarding claim 9, Iwata et al. teach the device comprises an n-type metal oxide semiconductor field effect transistor (NMOSFET).

Regarding claim 10, Iwata et al. teach the NMOSFET comprises a gate electrode (102) formed over a channel region (106), and wherein the n-type source/drain buffer region (105) separates the n-type source/drain main region (108) from the channel region (106).

Regarding claim 11, Iwata et al. differ from the claimed invention by not showing the substrate comprises monocrystalline silicon. It would have been obvious to one having ordinary skill in the art at the time the invention was made for the substrate comprises monocrystalline silicon because it has high electron mobility of device.

Since the arsenic ions are doped into the monocrystalline silicon substrate, the arsenic ion implanted region inherently comprises an amorphous silicon region.

Regarding claim 12, Iwata et al. teach a p-n junction formed at a first interface between the channel region (106) and the buffer region (105) is separated from a second interface between the amorphous silicon region (108) and the monocrystalline silicon.

Regarding claim 13, it is inherent that point defects generated by the implanting phosphorous ions are absorbed by the amorphous silicon, such that diffusion of the phosphorous ions during the heat-treating is suppressed.

Regarding claim 15, Iwata et al. differ from the claim invention by not showing the first acceleration energy level comprises about 10 keV or less. It would have been obvious to one having ordinary skill in the art at the time the invention was made for the first acceleration energy level comprises about 10 keV or less in order to reduce the reverse short channel effect. Furthermore, it has been held that where the general conditions of a claim are disclosed in the prior art, discovering the optimum or workable ranges involve only routine skill in the art. In re Aller, 105 USPQ 233.

Regarding claim 16, Iwata et al. teach the heat-treating step comprises heat-treating at about 1000^0 C for about 10 seconds (column 12, line 41).

Regarding claim 17, Iwata et al. differ from the claimed invention by not showing an arsenic concentration in the n-type source/drain main region is between $1x10^{20}/cm^2$ and $5x10^{21}/cm^2$ and a phosphorous concentration in the n-type source/drain buffer region is between $1x10^{18}/cm^2$ and $5x10^{19}/cm^2$. It would have been obvious to one having ordinary skill in the art at the time the invention was made for an arsenic concentration in the n-type source/drain main region is between $1x10^{20}/cm^2$ and $5x10^{21}/cm^2$ and a phosphorous concentration in the n-type source/drain buffer region is between $1x10^{18}/cm^2$ and $5x10^{19}/cm^2$ in order to reduce the reverse

short channel effect. Furthermore, it has been held that where the general conditions of a claim are disclosed in the prior art, discovering the optimum or workable ranges involve only routine skill in the art. In re Aller, 105 USPQ 233.

Regarding claim 22, Iwata et al. (figure 1) teach a method of manufacturing a semiconductor device, comprising:

forming extension regions (107) by implanting first arsenic ions in a semiconductor substrate; and

forming source/drain regions (108) and buffer regions (105) extending beyond the source/drain regions (108), comprising:

implanting phosphorous ions in the arsenic ion implanted regions at an acceleration energy level (column 10, line 66 – column 11, line 3) lower than the acceleration energy level for implanting the second arsenic ions (column 11, lines 8-15).

Since the acceleration energy level (50 keV) of the arsenic ions is greater than the acceleration energy level (30keV) of the phosphorous ions, the concentration peak of the phosphorous ions would locate in the arsenic ion implanted regions.

performing a heat treatment to active the arsenic ions in the arsenic ion implanted regions and the phosphorous ions (column 10, line 66 – column 12, line 45).

Iwata et al. differ from the claimed invention by not showing the second arsenic ions at acceleration energy, which is no greater than 15keV. The energy of implanting arsenic ions is a known variable, which is subject to routine experimentation and optimization. Wu teach the implanting arsenic ions at the acceleration energy about 5 to 150keV (column 4, lines 42-48), which is in the claimed range. It would have been obvious to one having ordinary skill in the art

at the time the invention was made for the first acceleration energy is no greater than 15keV in order to reduce the reverse short channel effect. Furthermore, it has been held that discovering an optimum value of a result effective variable involves only routine skill in the art. In re Boesch, 617 F.2d 272, 205 USPQ 215 (CCPA 1980).

Iwata et al. and Wu differ from the claimed invention by not showing implanting phosphorous ions in the arsenic ion implanted regions at an acceleration energy level, which is no greater than 10 keV. It would have been obvious to one having ordinary skill in the art at the time the invention was made for implanting phosphorous ions in the arsenic ion implanted regions at an acceleration energy level, which is no greater than 10 keV in order to reduce the reverse short channel effect. Furthermore, it has been held that discovering an optimum value of a result effective variable involves only routine skill in the art. In re Boesch, 617 F.2d 272, 205 USPQ 215 (CCPA 1980).

Response to Arguments

Applicant's arguments filed 09/08/04 have been fully considered but they are not persuasive.

It is argued, in page 9 of the remarks, that Khouja is direct to a method of computing the power dissipated in a digital circuit, and the combined references are unrelated. This argument is not convincing because there is no combined references such as Khouja in the office action.

It is argued, in page 10 of the remarks, that Iwata et al. and Wu do not teach or suggest implanting phosphorous after implanting arsenic. This argument is not convincing because the

applicant does not clarify why does the phosphorous need to be implanted after arsenic in the claimed invention. However, the combined device (Iwata et al. and Wu) shows the implanting phosphorous after implanting arsenic for the reasons that are discussed above.

It is argued, in page 12, that Iwata et al. and Wu do not teach or suggest the claimed invention, which may suppress the reverse channel effect. This argument is not convincing because the applicant does not show suppressing the reverse channel effect in the claimed limitations.

Conclusion

Any inquiry concerning this communication or earlier communications from the examiner should be directed to Quang D Vu whose telephone number is 571-272-1667. The examiner can normally be reached on Monday-Friday.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Eddie Lee can be reached on 571-272-1732. The fax phone number for the organization where this application or proceeding is assigned is 703-872-9306.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free).

qv
November 10, 2004

Sara W Crane
Sara Crane
Primary Examiner